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TRX_120_067
120-GHz Highly Integrated IQ Transceiver with Antennas in Package in Silicon Germanium Technology

Data Sheet

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<th>Date:</th>
<th>Author:</th>
<th>Filename:</th>
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<td>14-Mar-2023</td>
<td>Silicon Radar GmbH</td>
<td>Datasheet_TRX_120_067_V0.5</td>
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## Version Control

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<td>Template, contents</td>
<td>Initial release</td>
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<td>0.2</td>
<td>8 Measurement Results</td>
<td>Scale in figures 20 and 21 corrected</td>
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<tr>
<td>0.3</td>
<td>6.3 Evaluation Kit</td>
<td>Information regarding to SR's new SiRad Easy® r4 platform</td>
</tr>
<tr>
<td>0.4</td>
<td>4.4 Electrical Characteristics, 7 Reliability and Environmental Test</td>
<td>Notation of 'IQ amplitude imbalance' (Aimb) notation corrected. Status of all tests listed in Table 7 updated.</td>
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<td>0.5</td>
<td>5.1 Outline Dimensions, 8 Measurement Results</td>
<td>Figure 4, Position of Antenna Arrays... : Mold cap dimension corrected, and cross section added. Figure 8, Current Consumption vs. Temperature, and figure 16, TX Output Frequency vs. Temperature: shown temperature range extended.</td>
</tr>
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1 Features

- Radar front end (RFE) with antennas in package for 122-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 380 mW in continuous operating mode
- Duty cycling is possible
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- RX and TX patch antennas
- Wide bandwidth of up to 6 GHz
- QFN56 leadless plastic package 8 × 8 mm²
- Package partly molded, MSL3 rated
- Pb-free, RoHS compliant package
- Replaces the TRX_120_001

1.1 Overview

The RFE is an integrated transceiver circuit for the 122-GHz ISM band with antennas in package. It includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage-controlled oscillator, divide-by-32 outputs and transmit and receive antennas (see Figure 1). The RF signal from the oscillator is directed to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature LO signal. The 120-GHz VCO has four analog tuning inputs with different tuning ranges and tuning slopes. The tuning inputs can be combined to obtain a wide frequency tuning range. The analog tuning inputs together with integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs.

The IC is fabricated in a SiGe BiCMOS technology.

1.2 Applications

The main field of application for the 120-GHz transceiver radar frontend is in short range radar systems with a range up to about 10 meters. By using dielectric lenses or reflectors, the range can be increased considerably. The RFE can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of 6 GHz.
2 Block Diagram

Figure 1 Block Diagram
3 Pin Configuration

3.1 Pin Assignment

![Figure 2: Pin Assignment (QFN56, top view)]

3.2 Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - 6</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>divp</td>
<td>Divider outputs, positive and negative terminal, matched to 50 Ω load, DC coupled, external decoupling capacitor required.</td>
</tr>
<tr>
<td>8</td>
<td>divn</td>
<td>Reserved. Do not make any connections.</td>
</tr>
<tr>
<td>9, 10</td>
<td>X</td>
<td>Connect to ground.</td>
</tr>
<tr>
<td>11 - 14</td>
<td>GND</td>
<td>Reserved. Do not make any connections.</td>
</tr>
<tr>
<td>15</td>
<td>X</td>
<td>Reserved. Do not make any connections.</td>
</tr>
<tr>
<td>16</td>
<td>diven</td>
<td>Divider enable input: 1.2 V – enable, 0 – off. NMOS input, external pull-up resistor of 100 kΩ recommended.</td>
</tr>
<tr>
<td>17</td>
<td>pwr tx</td>
<td>Transmitter power control input: 1.2 V – full, 0 – -3 dB. NMOS input, external pull-up resistor of 100 kΩ recommended.</td>
</tr>
<tr>
<td>18</td>
<td>Vt3</td>
<td>VCO tuning input 3 (0 – VCC)</td>
</tr>
<tr>
<td>19</td>
<td>Vt2</td>
<td>VCO tuning input 2 (0 – VCC)</td>
</tr>
<tr>
<td>20</td>
<td>Vt1</td>
<td>VCO tuning input 1 (0 – VCC)</td>
</tr>
<tr>
<td>21</td>
<td>Vt0</td>
<td>VCO tuning input 0 (0 – VCC)</td>
</tr>
<tr>
<td>22</td>
<td>IF_Qp</td>
<td>IF Q output, positive terminal (DC coupled)</td>
</tr>
<tr>
<td>23</td>
<td>IF_Qn</td>
<td>IF Q output, negative terminal (DC coupled)</td>
</tr>
<tr>
<td>24</td>
<td>IF_In</td>
<td>IF I output, negative terminal (DC coupled)</td>
</tr>
<tr>
<td>25</td>
<td>IF_Ip</td>
<td>IF I output, positive terminal (DC coupled)</td>
</tr>
<tr>
<td>26</td>
<td>VCC</td>
<td>Supply voltage (3.3 V, 112 mA typ.)</td>
</tr>
<tr>
<td>27, 28</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>29, 30</td>
<td>GND</td>
<td>Ground pins, also connected to the exposed die attach pad.</td>
</tr>
<tr>
<td>31 - 56</td>
<td>NC</td>
<td>Not connected</td>
</tr>
<tr>
<td>57</td>
<td>GND</td>
<td>Exposed die attach pad of the QFN package, must be soldered to ground.</td>
</tr>
</tbody>
</table>
4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Remarks / Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>V_{CC}</td>
<td>-3.6</td>
<td>3.6</td>
<td>V to GND</td>
<td></td>
</tr>
<tr>
<td>DC voltage at tuning inputs</td>
<td>V_{VT}</td>
<td>-0.3</td>
<td>V_{CC} + 0.3</td>
<td>V</td>
<td>Inputs Vt0, Vt1, Vt2, Vt3</td>
</tr>
<tr>
<td>DC voltage at enable inputs</td>
<td>V_{EN}</td>
<td>-0.3</td>
<td>1.5</td>
<td>V</td>
<td>Inputs diven, pwr, tx</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>T_{J}</td>
<td>-50</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>T_{STG}</td>
<td>-50</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Floor life (out of bag) at factory ambient (30°C / 60% RH)</td>
<td>FL</td>
<td>-</td>
<td>168</td>
<td>h</td>
<td>IPC/JEDEC J-STD-033A MSL Level 3 Compliant ¹</td>
</tr>
<tr>
<td>ESD robustness</td>
<td>V_{ESD}</td>
<td>-</td>
<td>500</td>
<td>V</td>
<td>Human body model, HBM ²</td>
</tr>
</tbody>
</table>

¹ If the devices are stored outside of the packaging, beyond this time limit, the device should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 12 hours.

² CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Remarks / Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient temperature</td>
<td>T_{A}</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
<td>V_{CC}</td>
<td>3.13</td>
<td>3.47</td>
<td>V</td>
<td>(3.3 V ± 5%)</td>
</tr>
<tr>
<td>DC voltage at tuning inputs</td>
<td>V_{VT}</td>
<td>0</td>
<td>V_{CC}</td>
<td>V</td>
<td>Inputs Vt0 – Vt3</td>
</tr>
<tr>
<td>DC voltage at enable inputs</td>
<td>V_{EN}</td>
<td>0</td>
<td>1.2</td>
<td>V</td>
<td>Inputs diven, pwr, tx</td>
</tr>
</tbody>
</table>

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Remarks / Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance, junction-to-ambient</td>
<td>R_{thja}</td>
<td></td>
<td></td>
<td>30</td>
<td>K/W</td>
<td>JEDEC JESD51-5</td>
</tr>
</tbody>
</table>
4.4 Electrical Characteristics

\( T_A = -40^\circ \text{C} \) to +85°C unless otherwise noted. Typical values measured at \( T_A = 25^\circ \text{C} \) and \( V_{CC} = 3.3 \text{ V} \).

### Table 5 Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Remarks / Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply current consumption</td>
<td>( I_{CC} )</td>
<td>100</td>
<td>112</td>
<td>128</td>
<td>mA</td>
<td>TX on, CW mode</td>
</tr>
<tr>
<td>Enable input voltage, low level</td>
<td>( V_{EN,L} )</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
<td>Inputs diven, pwr_tx</td>
<td></td>
</tr>
<tr>
<td>Enable input voltage, high level</td>
<td>( V_{EN,H} )</td>
<td>0.9</td>
<td>1.2</td>
<td>V</td>
<td>Inputs diven, pwr_tx</td>
<td></td>
</tr>
<tr>
<td>VCO tuning voltage</td>
<td>( V_{VT} )</td>
<td>0</td>
<td>( V_{CC} )</td>
<td>V</td>
<td>Inputs Vt0 – Vt3</td>
<td></td>
</tr>
<tr>
<td>RF Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO start frequency</td>
<td>( f_{TX_start} )</td>
<td>117.5</td>
<td>119.3</td>
<td>121.5</td>
<td>GHz</td>
<td>( Vt0 = Vt1 = Vt2 = Vt3 = 0 )</td>
</tr>
<tr>
<td>VCO stop frequency</td>
<td>( f_{TX_stop} )</td>
<td>123.5</td>
<td>125.8</td>
<td>128.0</td>
<td>GHz</td>
<td>( Vt0 = Vt1 = Vt2 = Vt3 = 3.3 \text{ V} )</td>
</tr>
<tr>
<td>VCO tuning full bandwidth</td>
<td>( \Delta f_{TX} )</td>
<td>5.9</td>
<td>6.2</td>
<td>6.8</td>
<td>GHz</td>
<td>( Vt0 – Vt3 ) interconnected</td>
</tr>
<tr>
<td>Number of adjustable frequency bands</td>
<td>( N )</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td>( Vt1 – Vt3 ) used for band switching</td>
</tr>
<tr>
<td>Pushing VCO</td>
<td>( \Delta f_{TX}/\Delta V_{CC} )</td>
<td>27</td>
<td></td>
<td></td>
<td>MHz/V</td>
<td></td>
</tr>
<tr>
<td>Phase noise</td>
<td>( P_N )</td>
<td>-90</td>
<td>-88</td>
<td></td>
<td>dBc/Hz</td>
<td>at 1 MHz offset</td>
</tr>
<tr>
<td>Transmitter output power</td>
<td>( P_{TX} )</td>
<td>-7</td>
<td>-3</td>
<td>1</td>
<td>dBm</td>
<td>Measured without antennas, ( V(pwr_tx) = 1.2 \text{ V} )</td>
</tr>
<tr>
<td>Divider ratio of TX signal</td>
<td>( N_{av} )</td>
<td></td>
<td>64</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Divider output power</td>
<td>( P_{av} )</td>
<td>-10</td>
<td>-7</td>
<td></td>
<td>dBm</td>
<td>Note 1</td>
</tr>
<tr>
<td>Divider output frequency</td>
<td>( f_{av} )</td>
<td>1.84</td>
<td>1.99</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>Receiver gain</td>
<td>( g_{RX} )</td>
<td>8</td>
<td>10</td>
<td></td>
<td>dB</td>
<td>Measured without antennas</td>
</tr>
<tr>
<td>IF frequency range</td>
<td>( f_{IF} )</td>
<td>0</td>
<td></td>
<td>200</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>IF output impedance</td>
<td>( Z_{OUT} )</td>
<td>500</td>
<td></td>
<td></td>
<td>( \Omega )</td>
<td>Differential outputs</td>
</tr>
<tr>
<td>IQ amplitude imbalance</td>
<td>( A_{imb} )</td>
<td>-1.5</td>
<td>-1.5</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>IQ phase imbalance</td>
<td>( P_{Himb} )</td>
<td>-10</td>
<td>10</td>
<td></td>
<td>deg</td>
<td></td>
</tr>
<tr>
<td>Noise figure (DSB)</td>
<td>( NF )</td>
<td>8.7</td>
<td></td>
<td></td>
<td>dB</td>
<td>Simulated, at ( f_{IF} = 1 \text{ MHz} )</td>
</tr>
<tr>
<td>Input compression point</td>
<td>1dB ICP</td>
<td>-20</td>
<td></td>
<td></td>
<td>dBm</td>
<td>Measured without antennas</td>
</tr>
</tbody>
</table>

Note 1: Measured single-ended. Divider outputs are loaded with 50 \( \Omega \), external decoupling capacitors are required. 50-\( \Omega \) match is not required in application.
5 Packaging

5.1 Outline Dimensions

![Outline Dimensions of QFN56, 0.5 mm Pitch, 8 mm × 8 mm](image)

5.2 Package Code

Top-Side Markings

TRX067

YYWW

5.3 Antenna Position

![Position of Antenna Arrays (top view) and Cross Section (through RX Antenna)](image)
### 6 Application

#### 6.1 Application Circuit Schematic

![Application Circuit Schematic](image)

**Figure 5** Application Circuit

#### 6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 µs and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

#### 6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: [https://www.siliconradar.com/evalkits/](https://www.siliconradar.com/evalkits/).

The **SiRad Easy® r4** platform supports development for many of Silicon Radar’s integrated IQ transceivers including radar front end boards for TRX.067. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.
6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds \( V_{CC} \) by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

![Equivalent I/O Circuits](image)

6.5 VCO Tuning Inputs

The VCO tuning inputs \( Vt0 - Vt3 \) are of analog nature but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby \( Vt3 \) has the widest tuning range, and \( Vt0 \) the narrowest.

<table>
<thead>
<tr>
<th>Input</th>
<th>VCO tuning bandwidth (MHz)</th>
<th>Middle band slope (MHz/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Vt0 )</td>
<td>( \Delta f_{TX,Vt0} )</td>
<td>720</td>
</tr>
<tr>
<td>( Vt1 )</td>
<td>( \Delta f_{TX,Vt1} )</td>
<td>750</td>
</tr>
<tr>
<td>( Vt2 )</td>
<td>( \Delta f_{TX,Vt2} )</td>
<td>1580</td>
</tr>
<tr>
<td>( Vt3 )</td>
<td>( \Delta f_{TX,Vt3} )</td>
<td>3450</td>
</tr>
</tbody>
</table>

The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the four tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and \( V_{CC} \)). The interconnection of all inputs \( Vt0 - Vt3 \) leads to the maximum tuning bandwidth. For example, if \( Vt0 \) is used as tuning input, the variation of the potential at \( Vt1, Vt2, Vt3 \) in all logical combinations of 0 and \( V_{CC} \), results in offsetting the tuning curve (see Figure 10).
7 Reliability and Environmental Test

<table>
<thead>
<tr>
<th>Qualification Test</th>
<th>JEDEC Standard</th>
<th>Condition</th>
<th>Pass/Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL3</td>
<td>J-STD-020E</td>
<td>Reflow simulation 3 times at 260°C</td>
<td>in progress</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>JESD22-A104</td>
<td>850 cycles at -40°C ... 125°C</td>
<td>pass</td>
</tr>
<tr>
<td>HTSL</td>
<td>JESD22-A103</td>
<td>1,000 h at 150°C</td>
<td>pass</td>
</tr>
<tr>
<td>HTOL</td>
<td>JESD22-A108</td>
<td>1,000 h at 85°C</td>
<td>pass</td>
</tr>
<tr>
<td>THB</td>
<td>JESD22-A101</td>
<td>1,000 h at 85°C and 85% RH</td>
<td>pass</td>
</tr>
</tbody>
</table>

Figure 7 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

\[ T_p \leq T_c = 260°C \]
\[ t_o \leq 30 \text{s} \]
\[ T_{s,\text{min}} = 150°C \]
\[ T_{s,\text{max}} = 200°C \]
\[ t_s = 60 \text{s} - 120 \text{s} \]
\[ T_l = 217°C \]
\[ t_l = 60 \text{s} - 150 \text{s} \]
\[ t_{25°C \text{-to-} T_p} \leq 480 \text{s} \]
8 Measurement Results

Figure 8  Current Consumption vs. Temperature

Figure 9  Measured Conversion Gain of the Receiver without antenna

Figure 10  VCO Tuning Curves. Vt0 is varied, while Vt1, Vt2 and Vt3 are driven high or low. For example, 011 means Vt3 = 0, Vt2 = 3.3 V, and Vt1 = 3.3 V.

Figure 11  Full Bandwidth VCO Tuning. Vt0, Vt1, Vt2, Vt3 are interconnected. (Vt0 = Vt1 = Vt2 = Vt3)

Figure 12  VCO Pushing - Vcc ± 300 mV
Vt0 = sweep, Vt1 = Vt2 = 0, Vt3 = 3.3 V

Figure 13  VCO Pushing - Full Bandwidth Operation. All tuning voltages, Vt0 = Vt1 = Vt2 = Vt3
Figure 14: Phase Noise of the Integrated Oscillator Measured at Divider Output (1.89 GHz)

Figure 15: VCO Pushing - Full Bandwidth Operation. All tuning voltages, Vt0 = Vt1 = Vt2 = Vt3

Figure 16: TX Output Frequency vs. Temperature

Figure 17: TX Output Power vs. Temperature (Normalized to 20°C)
The result of the measurements of the radiation patterns of TX and RX patch antennas at different frequencies are shown in Figure 20. The power levels are normalized separately for RX and TX measurements.
The combined normalized radiation patterns of RX and TX antenna for FMCW operation are shown in Figure 21. During the measurement, the IC was operated in FMCW mode with a bandwidth of 1 GHz. A corner reflector was used as the target. The frequency of the measurement refers to the start frequency of the sweep.

Figure 21  Combined Radiation Pattern of TX and RX Patch Antennas, measured in FMCW mode with 1-GHz modulation bandwidth at different frequencies – H-Plane (blue), E-Plane (orange)
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